# AIC HW2

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# Problem 1

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Corner | Temp  (°C) | Circuit | Waveform | Vout  (mV) | Ids  (A) | DC gain  (V/V) | Rout  (Ω) | Cin  (F) | Cout  (F) |
| TT | 25 | (b) | 一張含有 文字, 行, 繪圖, 螢幕擷取畫面 的圖片  自動產生的描述 | 726.117 | 42.4507u | -2.6400 | 7.3868k | 37.8985f | 47.3303f |
| TT | 0 | (a) | 一張含有 文字, 行, 螢幕擷取畫面, 繪圖 的圖片  自動產生的描述 | 945.275 | 17.5753u | -2.4806 | 10.2106k | 4.7420f | 42.1002f |
| TT | 25 | (a) | 一張含有 文字, 行, 繪圖, 螢幕擷取畫面 的圖片  自動產生的描述 | 918.353 | 20.6289u | -2.4679 | 9.8549k | 4.7640f | 42.1827f |
| TT | 75 | (a) | 一張含有 文字, 行, 繪圖, 圖表 的圖片  自動產生的描述 | 870.359 | 26.1780u | -2.4174 | 9.4633k | 4.7856f | 42.3225f |
| FF | 25 | (a) | 一張含有 文字, 繪圖, 行, 圖表 的圖片  自動產生的描述 | 854.429 | 33.0366u | -2.6042 | 7.6539k | 4.8411f | 42.4229f |
| SS | 25 | (a) | 一張含有 文字, 行, 繪圖, 圖表 的圖片  自動產生的描述 | 982.866 | 11.5971u | -2.2322 | 13.4338k | 4.7264f | 41.9959f |
| FnSp | 25 | (a) | 一張含有 文字, 行, 繪圖, 螢幕擷取畫面 的圖片  自動產生的描述 | 845.718 | 25.5978u | -2.6229 | 9.0640k | 4.6852f | 42.4630f |
| SnFp | 25 | (a) | 一張含有 文字, 行, 繪圖, 圖表 的圖片  自動產生的描述 | 992.596 | 16.0392u | -2.2991 | 10.9135k | 4.8468f | 41.9022f |

# Code for Problem 1

1. \*\*\*-----------------------\*\*\*

2. \*\*\*        setting        \*\*\*

3. \*\*\*-----------------------\*\*\*

4. .lib "~/U18\_HSPICE\_Model/mm180\_reg18\_v124.lib" tt

5. .TEMP 25

6. .op

7. \*\*\*-----------------------\*\*\*

8. \*\*\*       simulation      \*\*\*

9. \*\*\*-----------------------\*\*\*

10. .option post

11. .option captab

12. .tf V(Vout) Vinput

13. .tran 0.01u 60u

14. .probe id\_mos = I(MN)

15.

16. \*\*\*-----------------------\*\*\*

17. \*\*\*      parameters       \*\*\*

18. \*\*\*-----------------------\*\*\*

19. .param wn = 6u

20. .param ln = 0.9u

21. .param wp = 5u

22. .param lp = 1u

23. .global VDD GND

24.

25. \*\*\*-----------------------\*\*\*

26. \*\*\*      power/input      \*\*\*

27. \*\*\*-----------------------\*\*\*

28. Vsupply VDD GND 1.8v

29. \*              SIN(Offset   Amplitude   Freq.   Delay )

30. Vinput Vin GND SIN(0.6V     0.01V       100k    0)

31. \*\*\*-----------------------\*\*\*

32. \*\*\*        circuit        \*\*\*

33. \*\*\*-----------------------\*\*\*

34. MP  Vout    Vout    VDD     VDD    p\_18\_mm w=wp l=lp

35. MN  Vout    Vin     GND     GND    n\_18\_mm w=wn l=ln

36.

37. \*\*\*-----------------------\*\*\*

38. \*\*\*         alter         \*\*\*

39. \*\*\*-----------------------\*\*\*

40. .alter

41. .TEMP 0

42. .param wn = 2u

43. .param ln = 0.3u

44.

45. .alter

46. .TEMP 25

47. .param wn = 2u

48. .param ln = 0.3u

49.

50. .alter

51. .TEMP 75

52. .param wn = 2u

53. .param ln = 0.3u

54.

55. .end

# Problem 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Corner | Temp  (°C) | Circuit | Rout  (Ω) | Av  (V/V) |
| TT | 25 | (a) | 9.8549k | -2.4679 |
| TT | 25 | (b) | 7.3868k | -2.6400 |
| TT | 75 | (a) | 9.4633k | -2.4174 |
| TT | 75 | (b) | 7.6529k | -2.5072 |

**Relationship Between MOSFET Dimensions & Resistance:**

* The resistance difference between circuit (a) & (b) might be caused by short channel effects like velocity saturation. Velocity saturation occurs when the electric field in the channel becomes so strong that the carrier velocity (electrons or holes) reaches a maximum value and cannot increase further, despite increases in the electric field. This effectively increases the resistance of the channel. The effect is more pronounced in smaller MOSFETs. Therefore, even though 6μm/0.9μm & 2μm/0.3μm are of the same ratio, circuit (a) has higher .

**Temperature’s impact on MOSFETs:**

* + As temperature rises, more charge carriers are thermally generated, which reduces the voltage needed to form the conductive channel. This can lead to increased conduction (more current flow) at lower gate voltages. According to Sedra Smith’s Microelectronic Circuits, the magnitude of decreases by about 2mV per 1 °C rise in temperature. Reduced threshold voltage can shift the operating point of the MOSFET.
  + As for the gain, .

Both and typically decrease with temperature, this often results in a net decrease in voltage gain as temperature rises.

# Code for Problem 2

1. \*\*\*-----------------------\*\*\*

2. \*\*\*        setting        \*\*\*

3. \*\*\*-----------------------\*\*\*

4. .lib "~/U18\_HSPICE\_Model/mm180\_reg18\_v124.lib" tt

5. .TEMP 25

6. .op

7. \*\*\*-----------------------\*\*\*

8. \*\*\*       simulation      \*\*\*

9. \*\*\*-----------------------\*\*\*

10. .option post

11. .option captab

12. .tf V(Vout) Vinput

13. .tran 0.01u 60u

14. .probe id\_mos = I(MN)

15.

16. \*\*\*-----------------------\*\*\*

17. \*\*\*      parameters       \*\*\*

18. \*\*\*-----------------------\*\*\*

19. .param wn = 2u

20. .param ln = 0.3u

21. .param wp = 5u

22. .param lp = 1u

23. .global VDD GND

24.

25. \*\*\*-----------------------\*\*\*

26. \*\*\*      power/input      \*\*\*

27. \*\*\*-----------------------\*\*\*

28. Vsupply VDD GND 1.8v

29. \*              SIN(Offset   Amplitude   Freq.   Delay )

30. Vinput Vin GND SIN(0.6V     0.01V       100k    0)

31. \*\*\*-----------------------\*\*\*

32. \*\*\*        circuit        \*\*\*

33. \*\*\*-----------------------\*\*\*

34. MP  Vout    Vout    VDD     VDD    p\_18\_mm w=wp l=lp

35. MN  Vout    Vin     GND     GND    n\_18\_mm w=wn l=ln

36.

37. \*\*\*-----------------------\*\*\*

38. \*\*\*         alter         \*\*\*

39. \*\*\*-----------------------\*\*\*

40. .alter

41. .param wn = 6u

42. .param ln = 0.9u

43.

44. .alter

45. .TEMP 75

46. .param wn = 2u

47. .param ln = 0.3u

48.

49. .alter

50. .TEMP 75

51. .param wn = 6u

52. .param ln = 0.9u

53.

54. .end

# Problem 3

一張含有 行, 繪圖, 螢幕擷取畫面, 文字 的圖片

自動產生的描述

Fig 1. Circuit(a) - Curve at Temperatures 0 ~ 80 °C

一張含有 行, 螢幕擷取畫面, 繪圖, 文字 的圖片

自動產生的描述

Fig 2. Circuit(b) - Curve at Temperatures 0 ~ 80 °C

* increases very slightly with temperature at lower but decreases with temperature at higher . Let first examine how temperature affects electrons/holes. Temperature has 2 effects on carriers:

1. Higher temperatures can increase the number of carriers through thermal generation. This is likely what leads to the decrease in as mentioned in problem 2.
2. Carrier mobility typically decreases with temperature due to increased lattice vibrations (phonon scattering).

* I believe that at lower . the effect of increasing carrier concentration takes dominance, and higher temperatures allow more current to flow through. However, at higher , the slowing effect is more dominant. Increased lattice vibrations lead to more frequent collisions between carriers and the crystal lattice, so the higher the temperature, the less the current.

# Code for Problem 3

1. \*\*\*-----------------------\*\*\*

2. \*\*\*        setting        \*\*\*

3. \*\*\*-----------------------\*\*\*

4. .lib "~/U18\_HSPICE\_Model/mm180\_reg18\_v124.lib" tt

5. .TEMP T

6. .op

7. \*\*\*-----------------------\*\*\*

8. \*\*\*       simulation      \*\*\*

9. \*\*\*-----------------------\*\*\*

10. .option post

11. .DC Vgs  0V 1.8V 0.05V sweep T 0 80 10

12. .probe id\_mos = I(MN)

13.

14. \*\*\*-----------------------\*\*\*

15. \*\*\*      parameters       \*\*\*

16. \*\*\*-----------------------\*\*\*

17. .param wn = 6u

18. .param ln = 0.9u

19. .param wp = 5u

20. .param lp = 1u

21. .global VDD GND

22.

23. \*\*\*-----------------------\*\*\*

24. \*\*\*      power/input      \*\*\*

25. \*\*\*-----------------------\*\*\*

26. Vsupply VDD GND 1.8v

27. \*              SIN(Offset   Amplitude   Freq.   Delay )

28. Vgs     Vin GND 1.8v

29. \*\*\*-----------------------\*\*\*

30. \*\*\*        circuit        \*\*\*

31. \*\*\*-----------------------\*\*\*

32. MP  Vout    Vout    VDD     VDD    p\_18\_mm w=wp l=lp

33. MN  Vout    Vin     GND     GND    n\_18\_mm w=wn l=ln

34.

35. .end